PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Craig BARRACK et al.

Application No.: 10/812,141

Filed: March 29, 2004

For: COMPACT PACKET SWITCHING NODE STORAGE ARCHITECTURE EMPLOYING DOUBLE DATA RATE SYNCHRONOUS DYNAMIC RAM

REQUEST FOR CORRECTED FILING RECEIPT

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Sir:

It is requested that a corrected filing receipt be issued reflecting the change shown below and on the attached copy thereof, namely:

the correct name of the second named inventor should be:

Yeong WANG

the correct Assignment for Published Patent Application should be:

Zarlink Semiconductor Inc., Kanata, Ontario, CANADA

Respectfully submitted,

June 15, 2004

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CERTIFICATE OF MAILING

I hereby certify that this correspondence and documents identified as being enclosed herewith are being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Missing Parts, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on **June 15, 2004.**

Ann Simonini

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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/812,141	03/29/2004	2818	770	23471	4	20	2

CONFIRMATION NO. 2157

FILING RECEIPT

OC000000012903092

24932
LAW OFFICE OF LAWRENCE E LAUBSCHER, JR
1160 SPA RD
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Date Mailed: 06/08/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

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Assignment For Published Patent Application

Zarlink Semiconductor ~~V.N.~~ Inc., ~~Irvine, CA,~~ KANATA, ONTARIO, CANADA

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 06/08/2004

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

Compact packet switching node storage architecture employing double data rate synchronous